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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/515,358	02/29/2000	Philip A Bourekas	M-7949US	1167

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EXAMINER
HUYNH, KIM T

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 08/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/515,358	Applicant(s) BOUREKAS, PHILIP A
	Examiner Kim Huynh	Art Unit 2181

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-4 and 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshioka et al. (U.S Patent 6,425,039)

Yoshioka discloses:

- A set of general purpose registers (fig.3), (col.8, lines 62-67)
- A set of exception registers that are switched for at least a subset of general purpose registers when an exception occurs. (col.5, lines 33-42)
- Set of exception registers is a dedicated set of registers for servicing exceptions. (col.8, lines 46-61)
- Set of exception registers is for servicing exceptions having a high priority. (col.13, lines 12-19)

- Processor provides a dedicated vector to set of exception registers (col.13, lines 63-67), (col.14, lines 1-13)
- A portion of set of exception registers is for servicing interrupts and another portion of set of exception registers is for servicing operating system calls. (col. 12, lines 59-67)
- Processor provides a first dedicated vector to software which uses portion of set of exception registers for interrupts and a second dedicated vector to software which uses another portion of set of exception registers for servicing operating system calls (col.12, lines 1-67), (col.1, lines 53-67)
- A select logic circuit having a first input terminal that receives an exception register active bit and a second input terminal that receives a register bit, said select logic circuit provides an output signal on an output terminal used to select between said set of general purpose registers and said exception registers. (col.14, lines 26-65), (col.18, lines 37-63)

3. Claims 9-12 and 16-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshioka et al. (U.S Patent 6,038,661)

Yoshioka discloses a method of interrupting the execution of a task and servicing an exception in a process comprising:

- Asserting an exception; (abstract, col.1, lines 31-36)
- Swapping a set of general registers for at least one set of exception registers (col.23, lines 30-40), (col.23, lines 11-21)

- Servicing exception using at least one set of exception registers (col.19, lines 40-46)
- Swapping out exception registers for set of general purpose registers and resuming execution of task (col.2, lines 12-19), (col.22, lines 46-60),(col.25, lines 13-25), (col.25, lines 37-46)
- At least one set of exception registers is dedicated set of exception registers (col.19, lines 25-38)
- Servicing exception using at least one set of exception registers comprises modifying the values of the registers in set of exception registers without disrupting the state of the interrupted task (col.23, lines 3-21), (col.25, lines 38-46)
- Exception is a high priority exception (fig.7), (col.13, lines 1-31) and (col.14, lines 1-67)
- Providing a first vector and activating at least one set of exception registers for high priority exception (col.22, lines 46-60), (col.19, lines 47-65)
- Providing a second vector and not activating set of exception registers for lower priority exceptions. (col.22, lines 46-60)

4. As for claims 16-18

Yoshioka further discloses:

- interrupting a task when an exception is asserted (col.25, lines 17-46)

- servicing exception without disrupting the state of the interrupted task (col.25, lines 17-46)
- resuming execution of interrupted task (col.25, lines 13-46)
- servicing comprises a means for activating at least one set of exception registers (col.25, lines 17-46), (col.28, lines 35-46)
- resuming execution interrupted task comprises deactivating exception registers and activating general purpose registers to resume execution of task (col.27, lines 1-62)
- activating comprises a first select logic circuit coupled to said set of general purpose registers and a second select logic circuit coupled to said at least one set of exception registers, said second select logic circuit receives an execution register active bit enabling said at least one set of exception registers and said second select logic circuit receives an inverted execution register active bit disabling set of general purpose registers (col.28, lines 17-34)

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

- Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka (U.S Patent 6,425,039)

  Yoshioka discloses the claimed inventions as discussed above for claims 1-4 and 6-8, which show processor comprising exception register. However, Yoshioka fails to show eight exception registers. The additions of more registers is a mere duplication of parts producing no new and unexpected result and therefore has no patentable significance. See MPEP 2144.04 VI B, and In re Harza, 274 F.2d 669, 124 USPQ 378(CCPA 1960). It would have been obvious to one of ordinary skill in the art the time of applicant's invention to include more registers into Yoshioka for a greater flexibility.

- Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al. (U.S Patent 6,038,661)

  Yoshioka discloses the claimed invention as discussed above for claims 9-12 and 16-18 except for the following:

- First vector is a dedicated vector and providing first vector automatically separates high priority exception from lower priority exceptions.
- Providing a first vector and activating at least a portion of exception registers for high priority exception when exception is an interrupt;
- Providing a second vector and activating at least another portion of exception registers for high priority exception when exception is an operating system call;
- Providing a third vector and not activating set of exception registers for lower priority exceptions
- First vector and second vector are dedicated vectors and providing first vector and providing second vector automatically separates high priority exception from lower priority exceptions

It would have been obvious to one having ordinary skill in the art at the time the invention was made to Yoshioka, since it has been held that omission of an element and its function in a combination where the remaining elements perform the same functions as before involves only routine skill in the art. *In re Karlson, 136 USPQ 184*

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384. The examiner can normally be reached on M-F 9am-7pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Peter Wong can be reached on (703)305-3477. The fax phone numbers for the organization where this application or proceeding is assigned are (703)746-7239 for regular communications and (703)746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

August 12, 2002

PETER WONG
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100